

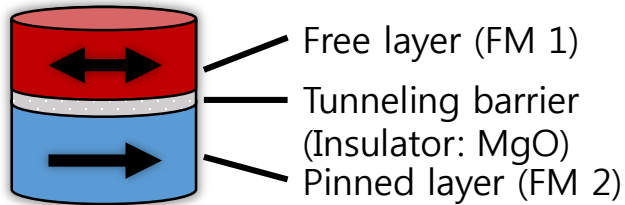
Magnetic tunnel junction beyond memory – from logic to neuromorphic computing

WANJUN PARK

DEPT. OF ELECTRONIC ENGINEERING, HANYANG UNIVERSITY

Magnetic Tunnel Junctions (MTJs)

- **Structure**



- **Function**

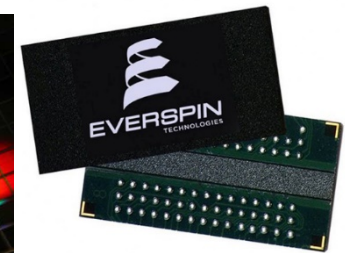
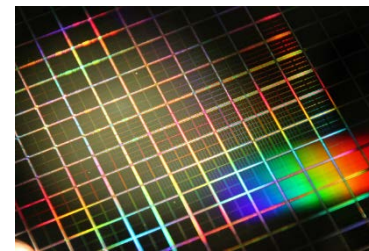
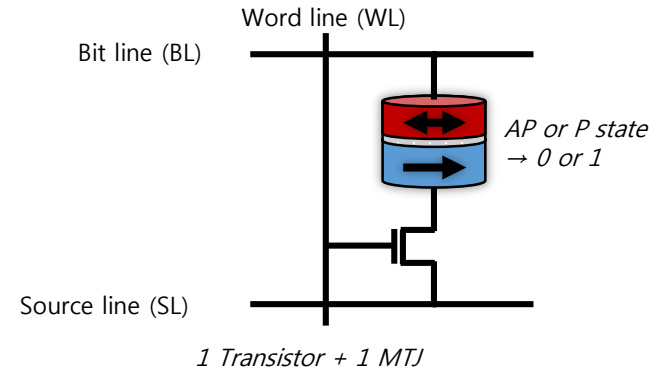
- ✓ Representation of non-volatile binary state according to magnetization configuration



- **Advantage**

- ✓ Scalability
- ✓ Low energy
- ✓ High speed
- ✓ High endurance
- ✓ CMOS compatibility

- **High density memory**



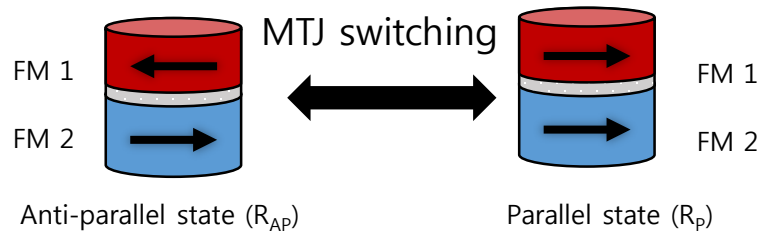
1GB STT-MRAM, Everspin (2016)

“ To find computing functions beyond memory from MTJ for integrated circuits”

- **Construction of 2-input MTJ**
- **MTJ Logic gates**
- **Neuromorphic computing**
 - Artificial MTJ neuron
 - Artificial MTJ synapse
 - Artificial Neurotransmission system

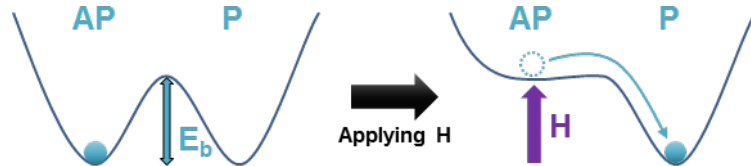
Basic configuration of MTJ

- Single input configuration for switching to achieve the binary state

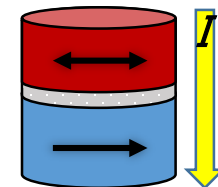
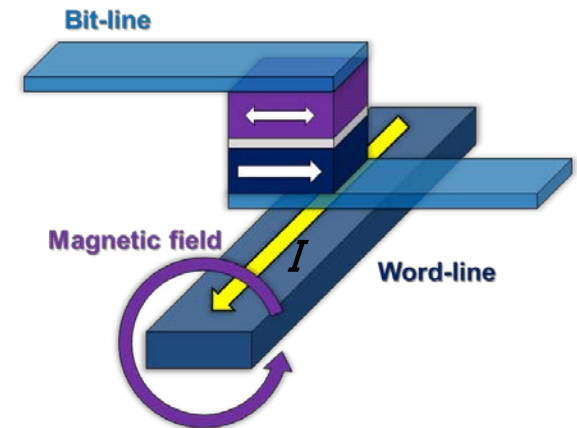
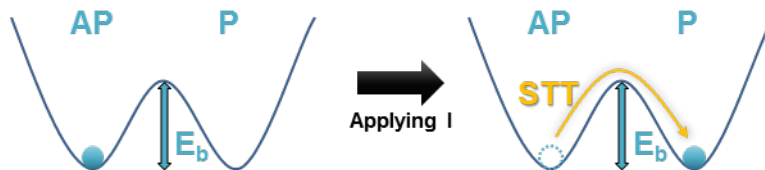


✓ Methods for magnetization reversal of free layer

- Switching variable 1: magnetic field switching (current induced Ampere field)



- Switching variable 2: Spin-transfer torque (STT) switching (spin polarized current)



Two-input configuration of MTJ

- **Motivation for multiple input extension**

“ Increase of functional flexibility”

- Reduction of switching stress by breakup of biases
- Increase of switching bias margin

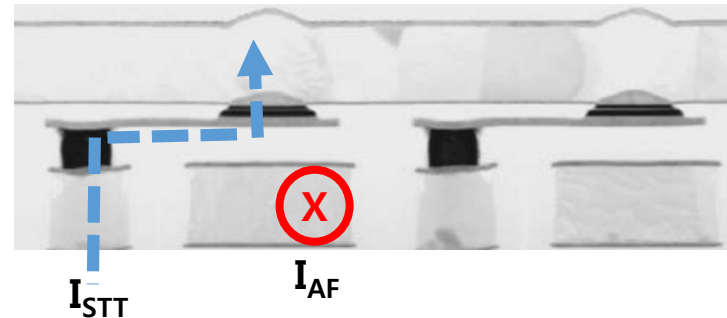
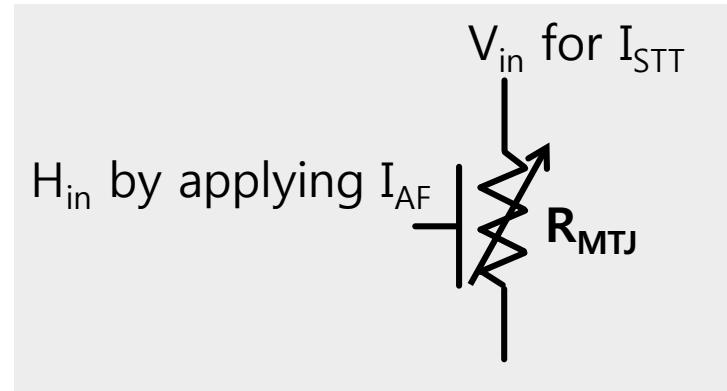
- **Physical variables for MTJ switching**

- Ampere field-induce switching
- Spin-transfer torque (STT) switching
- Thermally assisted switching (TAS)
- Voltage-assisted switching (ME effect)
- Spin-orbit torque (SOT) switching



Multiple input is available for MTJ

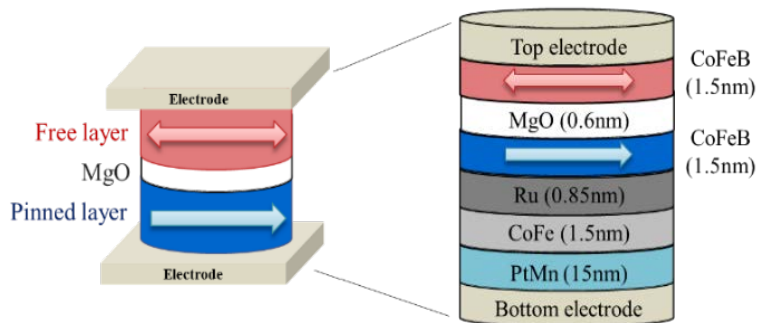
- **Our choice: STT & Ampere field for two switching inputs**
- **Sharing integration methods developed for MRAM**



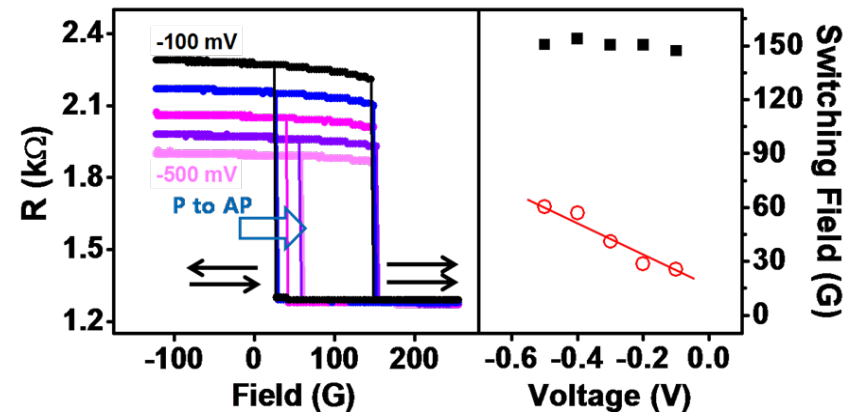
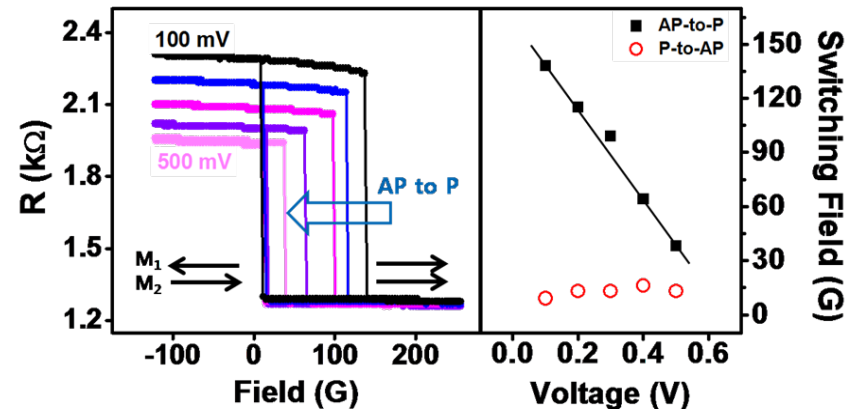
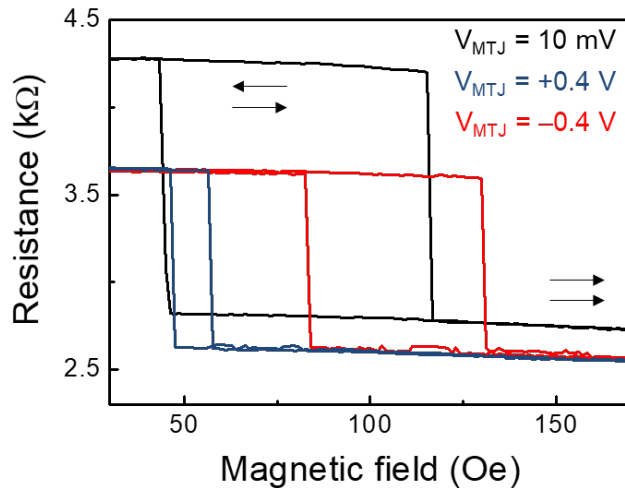
Structure of 2-input MTJ

Switching characteristics of 2-input MTJ

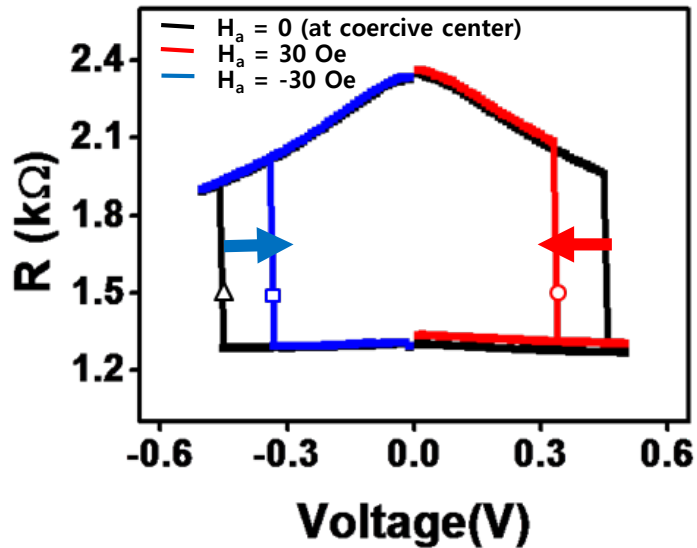
- MTJs for switching characteristics due to mixed inputs of STT & Ampere field



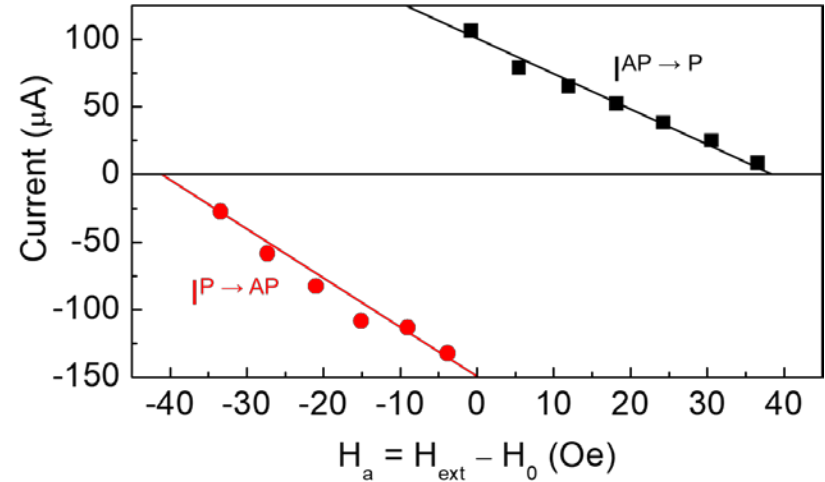
Size : $(80 \times 80) \sim (150 \times 600) \text{ nm}^2$



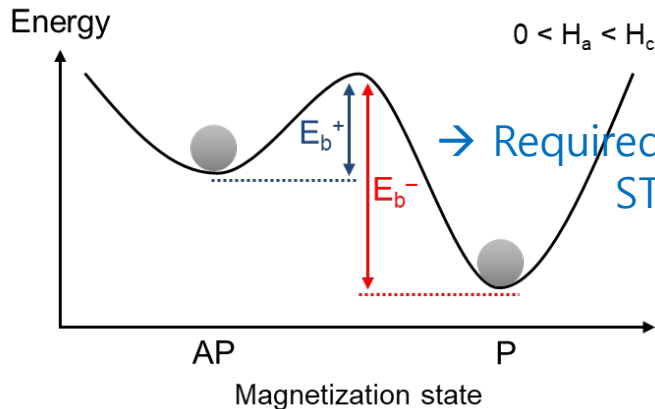
Interpretation of 2-input switching



“Magnetic field assisted STT switching”



- Case for switching to be P state



$$E_{b^+} = E_{b0} - E_b^*$$

Energy due to Ampere field ($H_{ext} = H_a$):

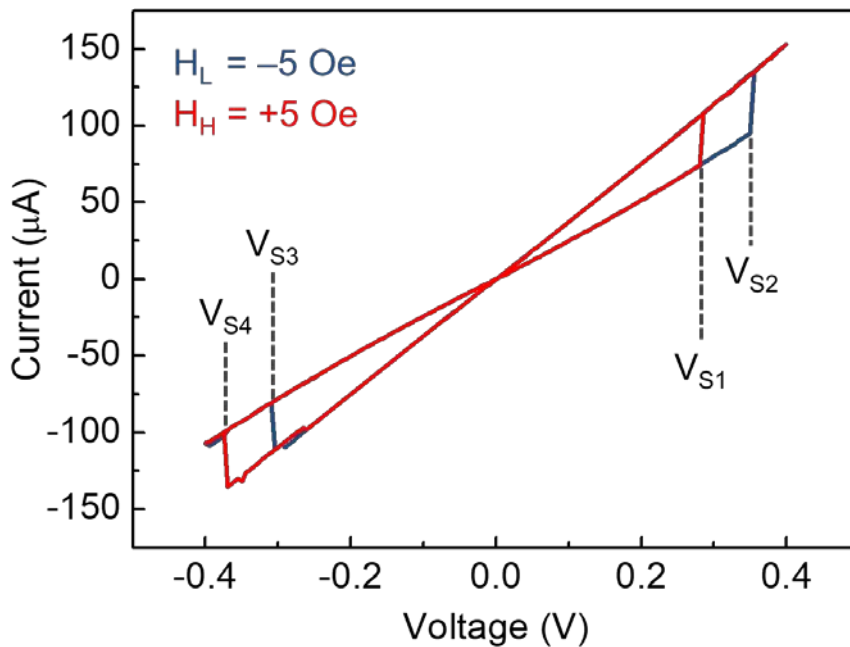
$$E_b^* = E_b(H_{ext}) \left(1 - \frac{a_J}{a_c} \right) = E_0 \left(1 - \frac{H_{ext}}{H_s} \right)^\beta \left(1 - \frac{a_J}{a_c} \right)$$

- H_s : Switching field
- E_0 : Energy barrier at zero magnetic field
- a_J : Spin transfer torque
- a_c : Critical spin transfer torque
- $\beta = 2$

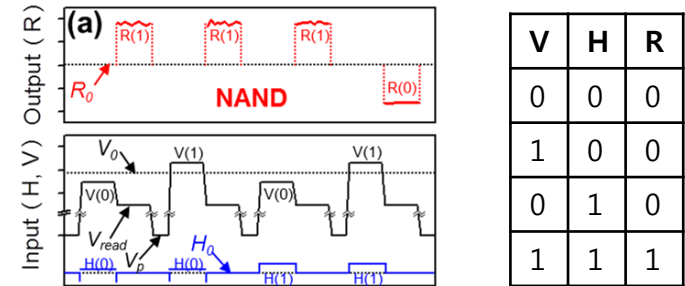
NAND/NOR representation

- Definition of binary states for each input

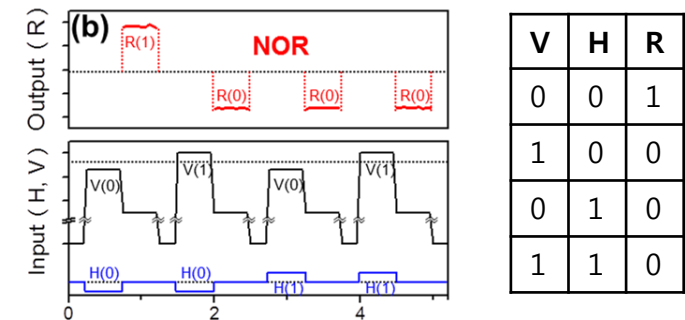
| Logic value | Input 1 (V) | Input 2 (H) | MTJ OUT |
|-------------|-------------|-------------|----------|
| 1 | V_H | H_H | R_{AP} |
| 0 | V_L | H_L | R_P |



- Assignment of input values to the STT input terminal



$V_L = 0.2 \text{ V} (< V_{S1}), V_H = 0.3 \text{ V} (V_{S1} < V_H < V_{S2})$
 $H_L = -5 \text{ (Oe)}, H_H = 5 \text{ (Oe)}$



$V_L = 0.3 \text{ V} (V_{S1} < V_L < V_{S2}), V_H = 0.4 \text{ V} (> V_{S2})$
 $H_L = -5 \text{ (Oe)}, H_H = 5 \text{ (Oe)}$

All logical representation founded in MTJ

- 7 Boolean logic representations from possible 12 binary inputs of voltage biases for the STT switching

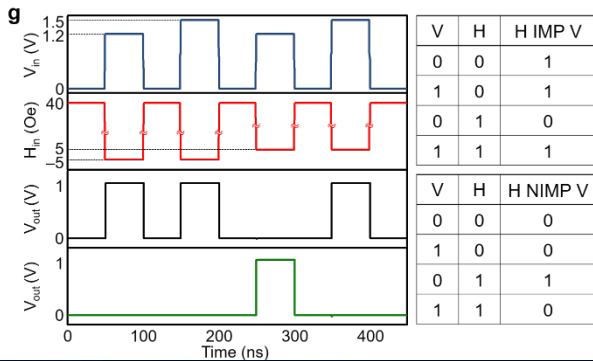
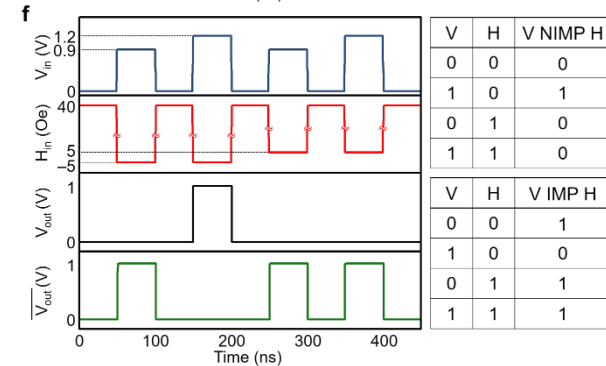
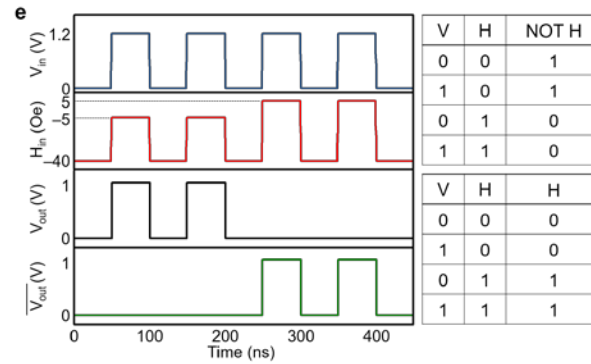
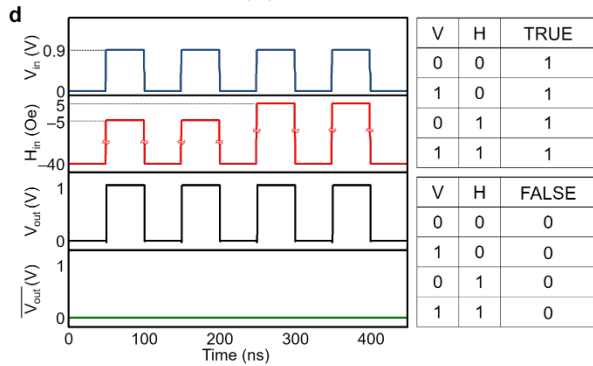
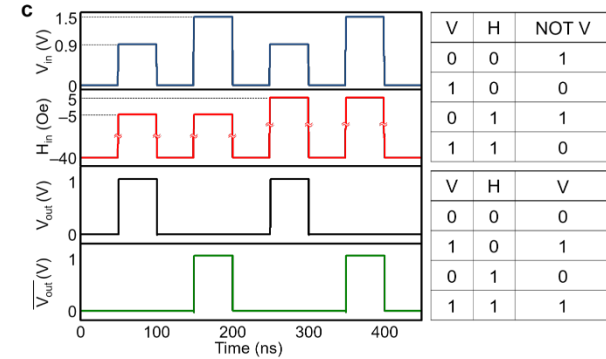
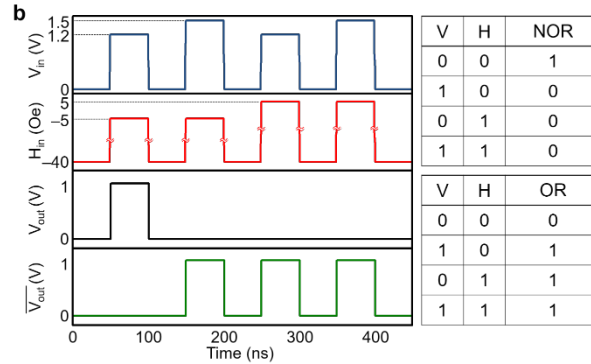
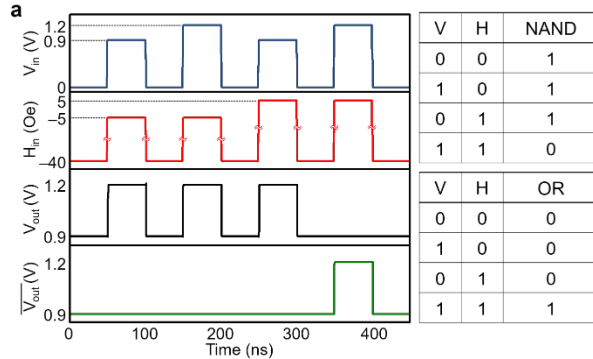
| No. | Initial State | Input set | | | | Input (V, H), Output (R) | | | | Logic function | |
|-----|-----------------|----------------|----------------|----------------|----------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|---|---|
| | | V _L | V _H | H _L | H _H | (V _L ,H _L) | (V _H ,H _L) | (V _L ,H _H) | (V _H ,H _H) | R _{AP} = 1, R _P = 0 | R _{AP} = 0, R _P = 1 |
| 1 | R _{AP} | 0.2 | 0.3 | -5 Oe | 5 Oe | R _{AP} | R _{AP} | R _{AP} | R _P | NAND | AND |
| 2 | | 0.3 | 0.4 | | | R _{AP} | R _P | R _P | R _P | NOR | OR |
| 3 | | 0.2 | 0.4 | | | R _{AP} | R _P | R _{AP} | R _P | NOT V | V |
| 4 | | 0.2 | 0.2 | | | R _{AP} | R _{AP} | R _{AP} | R _{AP} | TRUE | FALSE |
| 5 | | 0.3 | 0.3 | | | R _{AP} | R _{AP} | R _P | R _P | NOT H | H |
| 6 | | 0.3 | 0.3 | | | R _P | R _P | R _P | R _P | FALSE | TRUE |
| 7 | R _P | -0.25 | -0.35 | -5 Oe | 5 Oe | R _P | R _{AP} | R _P | R _P | V NIMP H | V IMP H |
| 8 | | -0.35 | -0.45 | | | R _{AP} | R _{AP} | R _P | R _{AP} | H IMP V | H NIMP V |
| 9 | | -0.25 | -0.45 | | | R _P | R _{AP} | R _P | R _{AP} | V NIMP H | V IMP H |
| 10 | | -0.25 | -0.25 | | | R _P | R _P | R _P | R _P | FALSE | TRUE |
| 11 | | -0.35 | -0.35 | | | R _{AP} | R _{AP} | R _P | R _P | NOT H | H |
| 12 | | -0.45 | -0.45 | | | R _{AP} | R _{AP} | R _{AP} | R _{AP} | TRUE | FALSE |

MTJ Logic gate

- **Logic gate for digital computing**
 - Cascading computing

Full schematic of a logic gate

14 Boolean functions computed in MTJ logic gate

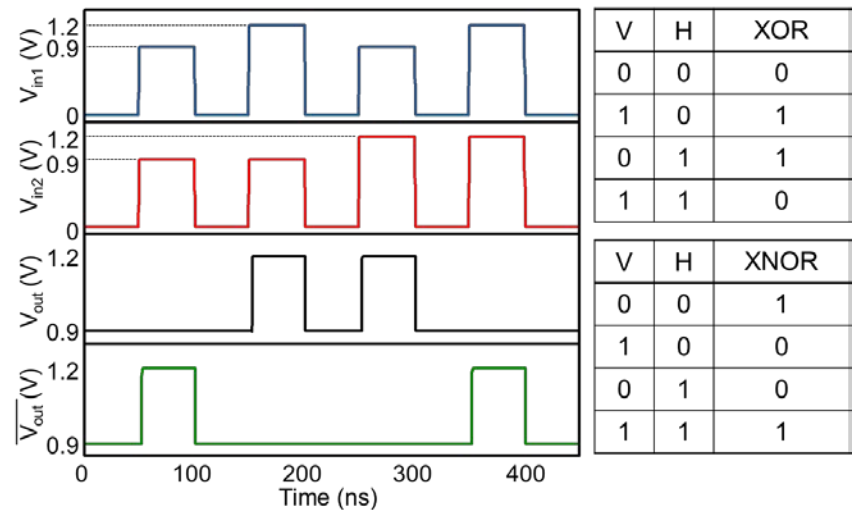


- Each function is confirmed by SPICE simulation modified with MTJ micro-model

- XOR and XNOR are missing among full 16 Boolean logics

XOR/XNOR MTJ Logic gate

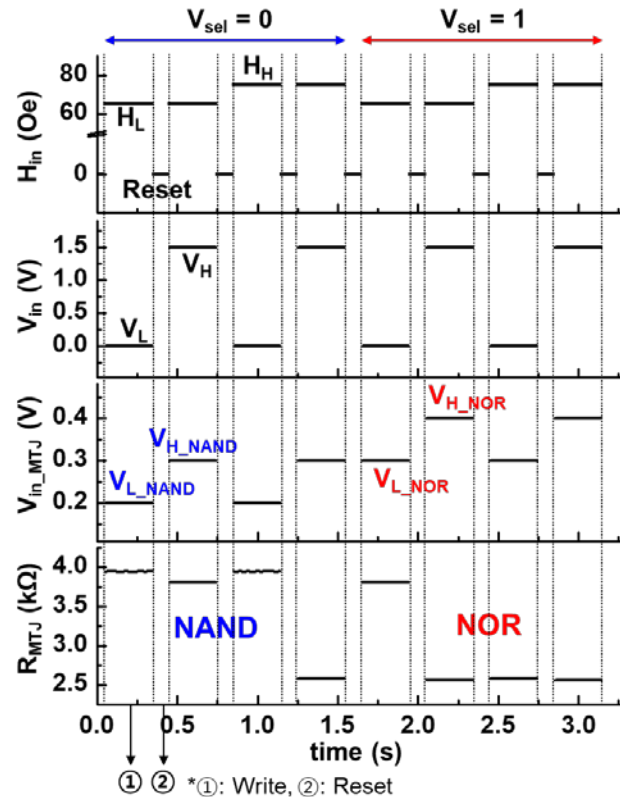
- XOR/XNOR gate could be completed by using "cascading computing"



- Conclusively, we have two types of MTJ logic gate which allow any digital computing

Reconfigurable Logic

- Reconfigurability: further advantage of MTJ logic

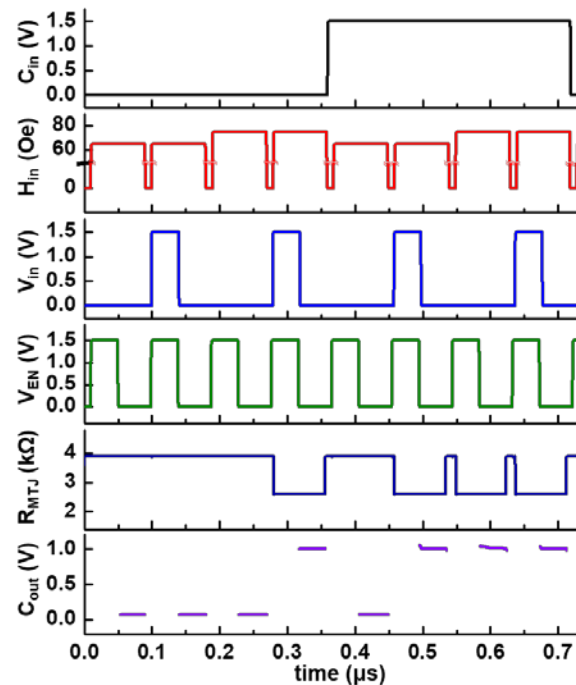


| H_{in} | V_{in} | V_{sel} | V_{in_MTJ} | R_{MTJ} | |
|----------|----------|-----------|---------------|-----------|---------------------------|
| 0 | 0 | 0 | V_{L_NAND} | 1 | "NAND" @ $V_{sel} = 0$ |
| 0 | 1 | 0 | V_{H_NAND} | 1 | |
| 1 | 0 | 0 | V_{L_NAND} | 1 | |
| 1 | 1 | 0 | V_{H_NAND} | 0 | |
| 0 | 0 | 1 | V_{L_NOR} | 1 | "NOR" @ $V_{sel} = 1$ |
| 0 | 1 | 1 | V_{H_NOR} | 0 | |
| 1 | 0 | 1 | V_{L_NOR} | 0 | |
| 1 | 1 | 1 | V_{H_NOR} | 0 | |

< Truth table >

Practical example for reconfigurable Logic

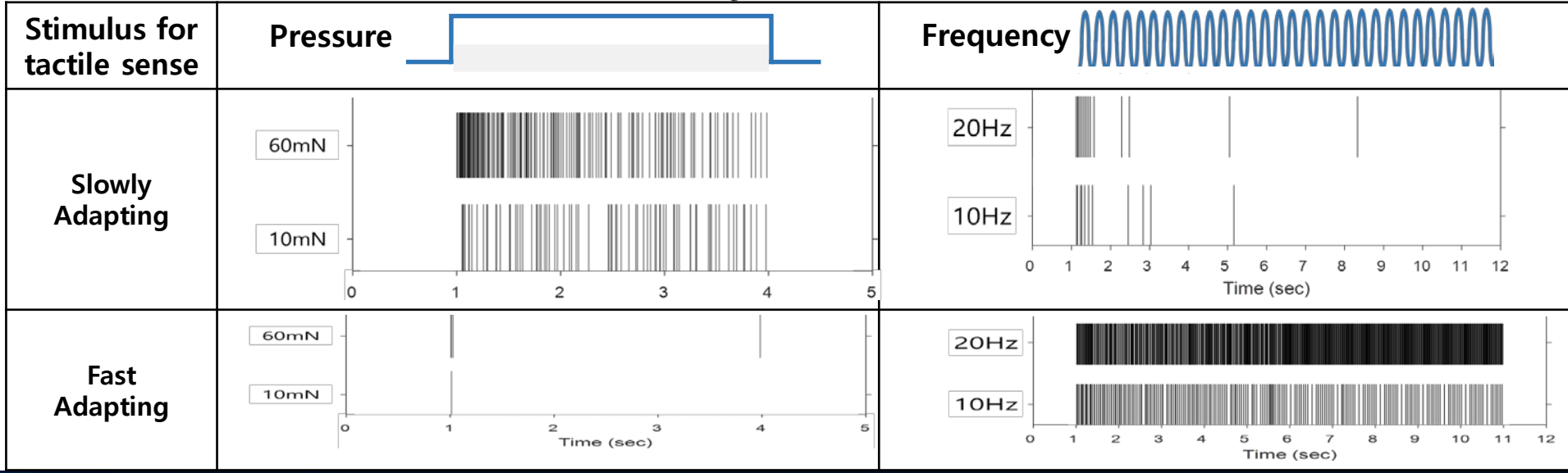
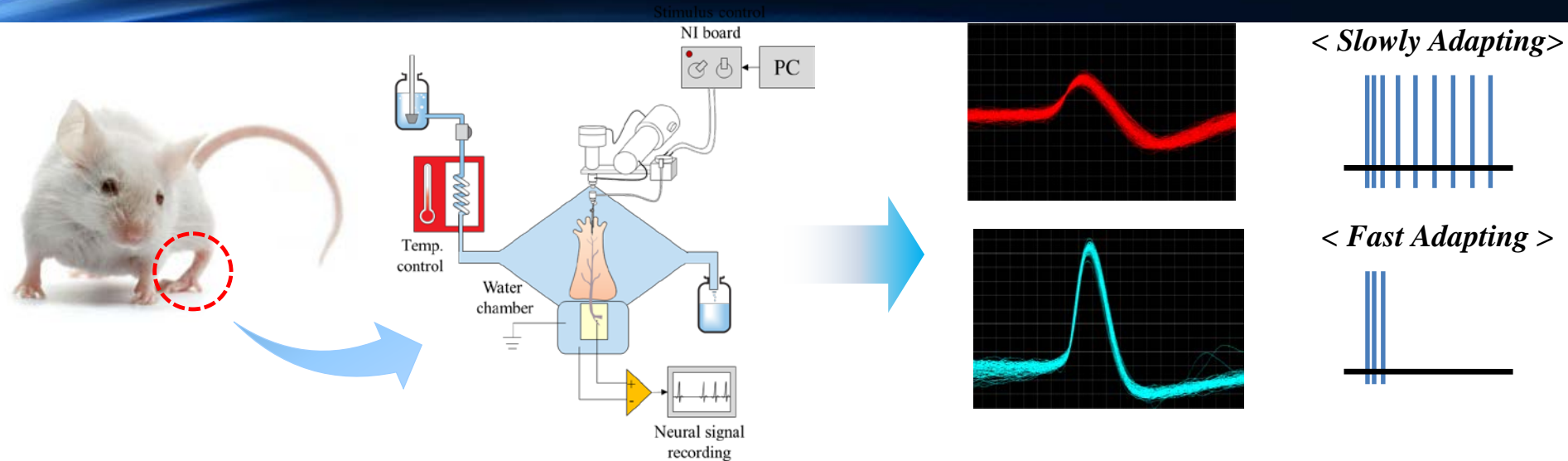
- Carry-out function with reconfigurable logic



| Input | | | Output | |
|-----------------|-----------------|-----------------|------------------|-------------------------------|
| H _{in} | V _{in} | C _{in} | C _{out} | |
| 0 | 0 | 0 | 0 | "AND" @ C _{in} =0 |
| 0 | 1 | 0 | 0 | |
| 1 | 0 | 0 | 0 | |
| 1 | 1 | 0 | 1 | |
| 0 | 0 | 1 | 0 | "OR" @ C _{in} =1 |
| 0 | 1 | 1 | 1 | |
| 1 | 0 | 1 | 1 | |
| 1 | 1 | 1 | 1 | |

< Truth table >

Neurotransmission – spike signal carrying information



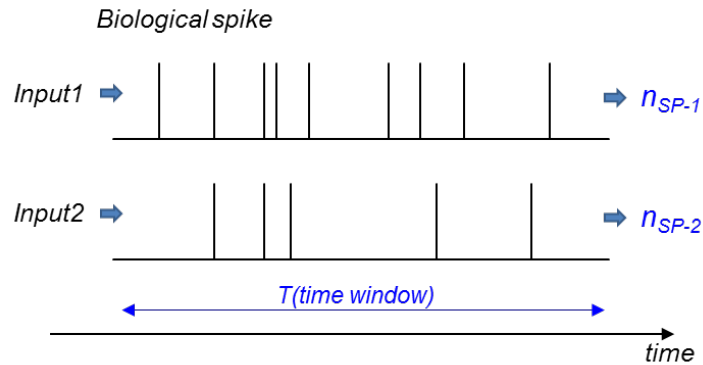
Neural coding

- **Neural (Biological) coding**

To find carrier for information according to "Strength and frequency" of input stimulus

- **Rate coding**

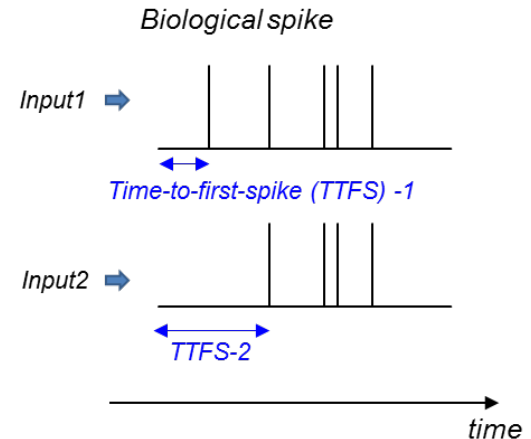
✓ **Information** → **spiking rate**



- **Temporal coding**

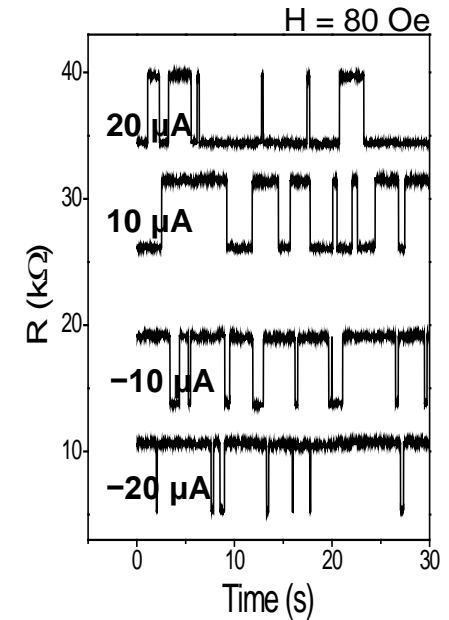
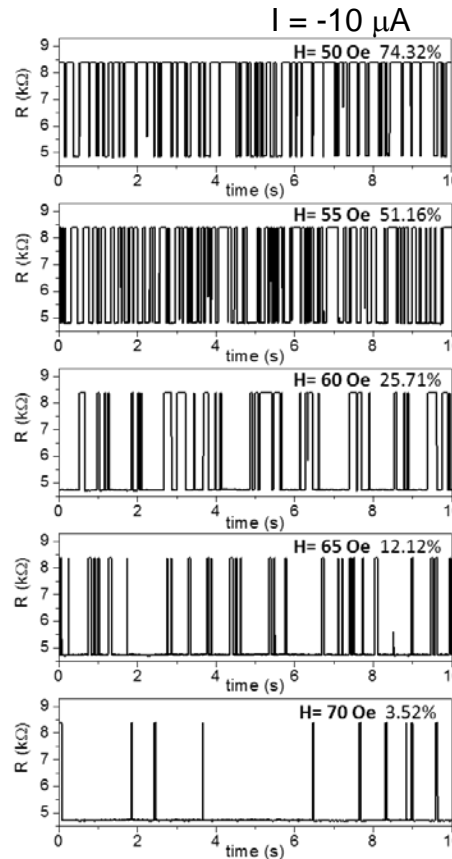
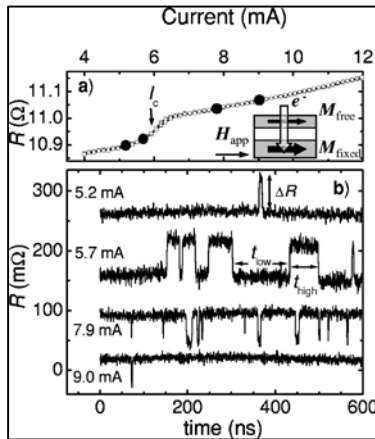
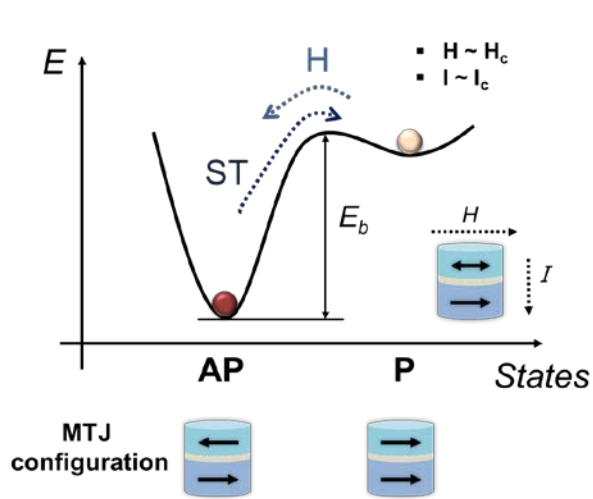
✓ **Information** → **Spiking pattern (Spike ordering in timing)**

- Time-to-first-spike, Phase Correlations, Spiking sequence, Synchrony etc.



Telegraphic switching

- Telegraphic switching by mixed effect of STT & Ampere field in 2-inpt MTJ

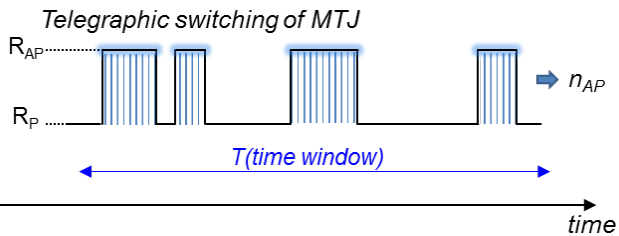
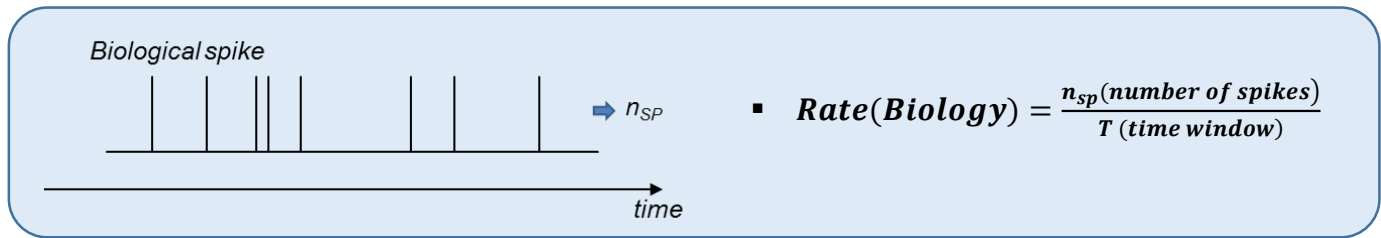


Total Energy ($E_M + E_{STT}$) $\sim E_S$
 \rightarrow Toggling between AP and P state
 Stochastic characteristic
 \rightarrow Switching probability $P(H, I)$ is defined as the carried information

M. Puffall et al., Phys. Rev. B (2004)

Rate coding

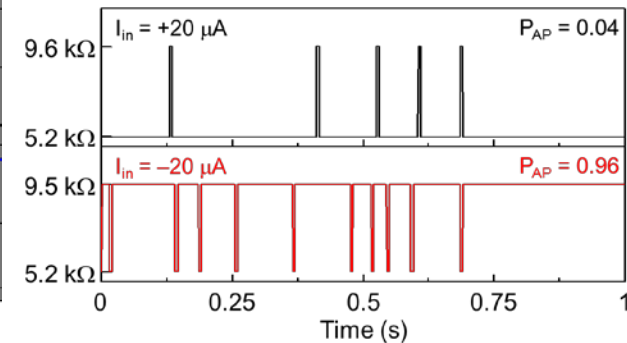
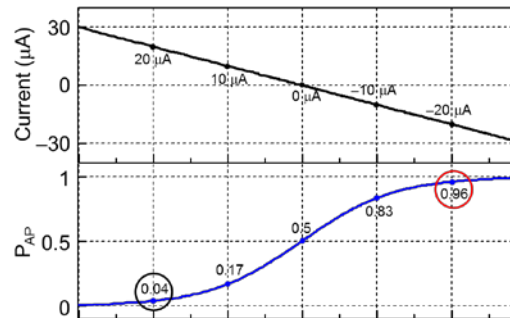
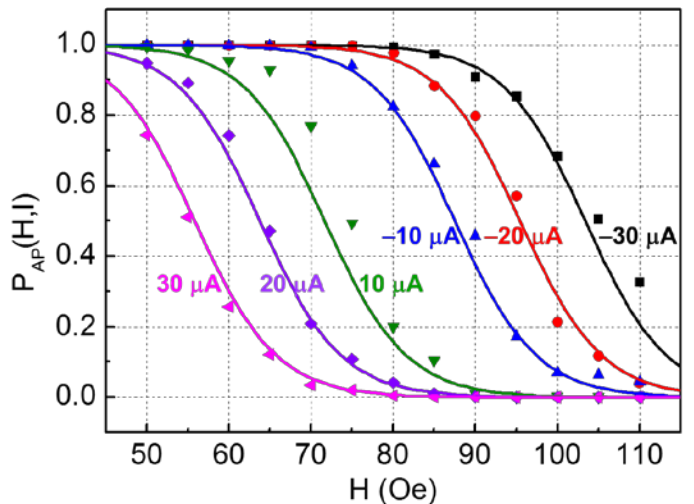
- Construction of neural coding : Rate coding



- Rate(MTJ) = $\frac{t_{AP}(\text{or } t_P)}{T(\text{total bit})}$ or $P_{AP}(H, I) = \frac{1}{1 + \exp(\alpha H + \beta I + \gamma)}$

Information carrier : rate

Stimulus : H and I applied by independent inputs

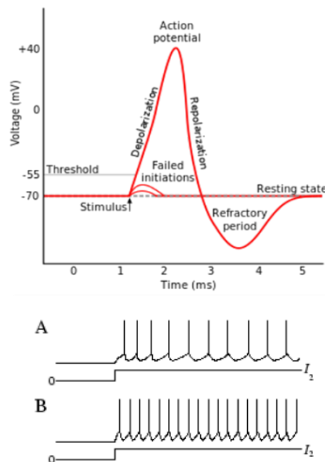
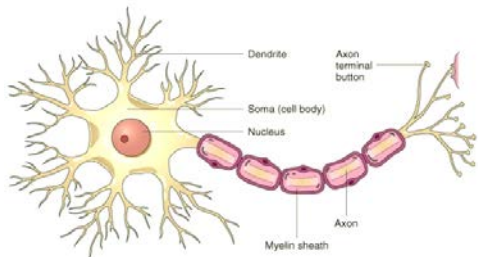


Artificial neuron function

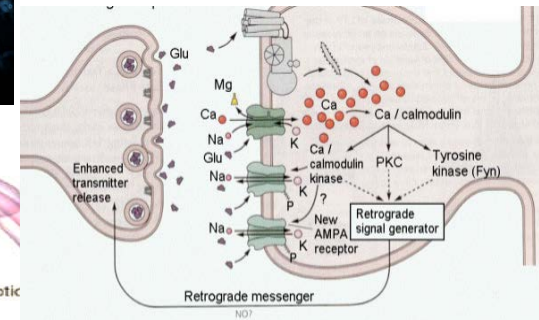
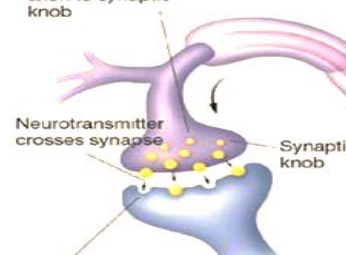
- **MTJ-based neuron architecture representing the rate coding**

Neurotransmission

- **Neuron system connected by "Synapse"**
(Spike-rate-dependent plasticity)



Signal travels along axon to synaptic knob



- **Spike(=Action potential) generation**
(when the signal is above threshold)

- **Neural coding**

- Information is coded through spike train
- Rate coding

- **Synaptic weight: plasticity for connection strength**

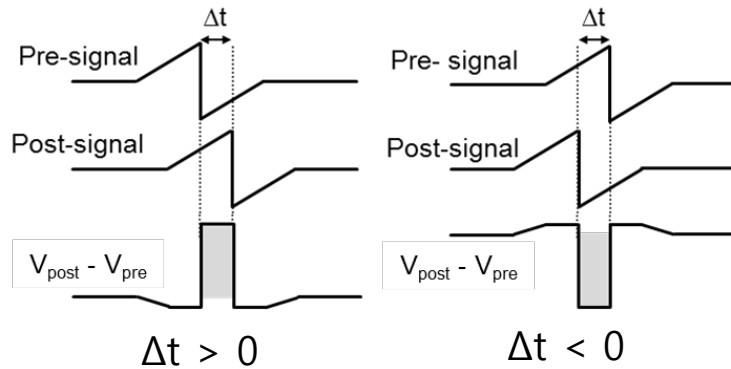
- **Weight modulation**

- Potentiation / Depression
- Spike-timing-dependent plasticity (STDP)

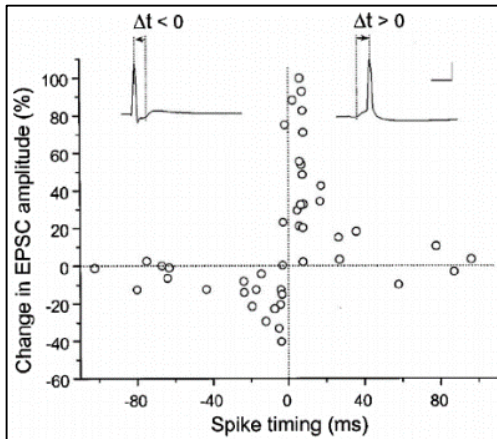
Memristive character of MTJ

MTJ-based artificial synapse

- Construction of input signal for “Spike-timing dependent plasticity”



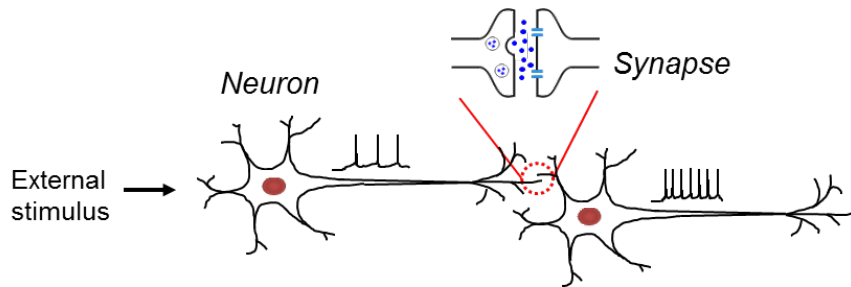
<Biological STDP>



R. Froemke et al., Nature (2002)

Artificial neurotransmission

- **Neurotransmission system**



- **Artificial neurotransmission system**

- MTJs are commonly used for neural and synaptic functions
- Learning rule of "**Spike-rate dependent plasticity**" is possibly applied

SRDP learning rule

Summary

- **MTJ was modified with two inputs for switching to achieve functional flexibility.**
- **Then we found various computing functions for digital to neuromorphic computing.**